WAVELET TRANSFORMATION ENGINE

ABSTRACT OF THE DISCLOSURE

An ASIC-implemented wavelet transformation engine (circuit) providing a wavelet filter is described. The wavelet filter itself provides up to a 9-stage FIR (finite impulse

5   response) filter with symmetrical coefficients. The architecture of the filter includes data inputs, a bank of shift registers (register bank), coefficient registers, a multiplier/accumulator, a sub-sampling component, and output (results) registers. The filter provides a wavelet-based compression solution that may be implemented in less-costly, page-based memory architecture (e.g., SDRAM), and does so in a manner that overcomes the inherent speed

10   disadvantage encountered due to the horizontal-optimized access strategy employed by page-based memory architectures.

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